

PATENT NUMBER

## U.S. UTILITY Patent Application

TH/2 O.I.P.E.

**PATENT DATE**

**SCANNED**

**Q.A**

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APPLICATION NO. 09/728441	CONT/PRIOR SUB D	CLASS 712	SUBCLASS 241	ART UNIT 2183	EXAMINER Chas. F. L. L.
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## APPLICANTS

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**अपराध**

Method and apparatus for modulo scheduled loop execution in a  
processor architecture

RECAP: (2)

PTO-2040  
12/89

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ISSUING CLASSIFICATION												
ORIGINAL				CROSS REFERENCE(S)								
CLASS		SUBCLASS		CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)							
INTERNATIONAL CLASSIFICATION												

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<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>			<b>CLAIMS ALLOWED</b>	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)			<b>NOTICE OF ALLOWANCE MAILED</b>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____	_____ (Primary Examiner) (Date)			<b>ISSUE FEE</b>	
				Amount Due	Date Paid
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner) (Date)			<b>ISSUE BATCH NUMBER</b>	

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